WEST

End of Result Set

Generate Collection Print

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- A common problem in display-oriented systems is the requirement to support migration from one display to its successor. If the successor is not a strict superset of its predecessor and if it is necessary to run programs written for the predecessor on the successor, then the hardware of the successor may have to be designed to support a "compatibility mode," which emulates the predecessor. This hardware may add significantly to the cost of the successor, or may constrain the design of the successor so as to prohibit the inclusion of useful characteristics. One approach to the migration problem is to repackage the predecessor display adapter with the successor. This inclusion of the predecessor adds significantly to the product cost. The concept disclosed herein is a "video compatibility feature," which allows a certain class of successor display adapters to operate in a cooperative manner with predecessor adapters. The successor adaptors must be of the display-processor frame-buffered type. Fig. 1 shows the relationship of the predecessor and the successor. The description below is with respect to the IBM PC Color Graphics card, it is understood that any adapter, including an adapter for TV, can be used. Digital video is generated by the Color Graphics card. The micro in the enhanced display adapter commands its "video compatibility feature" (VCF) to wait until a certain raster line of the picture comes from the Color Graphics card, and then to capture the digital video in a line buffer (Fig. 2). The micro then reads that line buffer, possibly reformats the data, and writes it into its frame buffer. The micro then captures another line of video and then another until the entire picture has been captured. Thus, the same picture can be made to appear on the CRT monitor of the enhanced display adapter as is currently appearing on the monitor connected to the Color Graphics card. Once the VCF is attached to the output of the Color Graphics card, the monitor for the Color Graphics card is no longer necessary because the picture will appear on the monitor attached to the enhanced display adapter. In fact, since the video from the Color Graphics card passes through the micro before being written into the frame buffer of the enhanced display adapter, useful transformations can be applied to it before display. In particular, the region of the screen in which the picture appears can be chosen arbitrarily. That region might be clipped, so that the picture could be overlaid with another picture, or the picture might appear on top of another picture. The picture might be blown up by writing a square region of 4 pixels (picture elements) for each pixel of the original picture, or the picture might be rotated 90 degrees, or some transformation of colors might be applied. The fact that the pixels of the picture emitted by the Color Graphics card are processed by the micro allows great flexibility in the resultant presentation. The purpose of the VCF is threefold: first to wait until the Color Graphics card emits a designated raster line of digital video, then to sample that digital video at predetermined sampling times, and then to buffer the sampled

digital video in a shift register (or FIFO (first- in, first-out)). If two such buffers are available in the VCF, then one raster line can be read out by the micro while another is being sampled. The fidelity of the sampled data depends on the mutual frequency and phase shift deviation between the VSF sampling clock (SCLK) and Color Graphics card videoclock (VCLK). The key is to establish the correct phase relationship between the sampling clock and the original video clock, at least at the beginning of each raster line. The SCLK clock can be derived from the VCLK if the latter is available from the common bus. In this case a phase shift between VCLK and SCLK should be either 0 or 180 degrees, and can be easily determined. If the VCLK clock is not available, a phase-locked loop system can be used (Fig. 3). The voltage-controlled oscillator (VCO) free-running frequency is chosen close to the VCLK frequency. The VCO frequency is used by a programmable sync generator to produce a SYNC signal analogous to the sync sequence of the Color Graphics card. Both sync sequences are compared by the phase comparator of a phase-locked loop. After the PLL acquisition time, the VCO frequency will be identical to VCLK with a fixed phase difference. The programmable sync generator (Fig. 4) consists of counter CNT, random access memory (RAM) and latch L. The CNT is needed if the RAM access time is longer than the VCO period. The output of CNT feeds the clock input of the L. The RAM address lines are connected to the outputs of L, and RAM input data is clocked in the L. The RAM is loaded by the micro during the initialization procedure. The VCF structure is shown in Fig. 5. The delay line has several taps. Which tap output is used as the sampling clock is determined by the control (CR) latch word. The selector (SEL) derives horizontal (HS) and vertical (VS) signals from the synchronization (SYNC) signal. The Line Counter (LCNT) counts HS, providing a current line number starting from the VS pulse. The micro writes the number of the line to be sampled into the vertical address (VA) latch and the number of the first pixel to be sampled into the horizontal address (HA) latch. If the LCNT and VA data are equal, the output of the comparator (COMP), multiplied by a blank signal, enables the sampling clock to shift M video data bits into the FIFO. For the Color Graphics card, M=4 (R, G, B and I). After the all L pixels of the video line have been sampled, the micro supplies a sequence of horizontal addresses to the HA latch. The WR pulse, writing a new horizontal address into the HA latch, also shifts data out of the FIFO. Hence, the FIFO data may be written into the Frame Buffer in DMA (direct memory access) mode. Not shown in Fig. 4 is the option for the micro to read pixel data from the FIFO so that it can be processed or transformed before it is written to the frame buffer. If two FIFOs are used in turn and several pixels are written in parallel in the Frame Buffer, then realtime frame sampling can be implemented. Proper phase difference between VCLK and SCLK is required to compensate for finite phase shift as a result of the phase-locked loop process and system propagation delays. This difference is resolved automatically during an initialization procedure. First, the host processor sends a special initialization image to the Color Graphics card (Fig. 6). The video information in this image will be recovered as digital information to adjust phase. The micro scans the phase by incrementing the CR contents between sampled video lines and checks the Cycle Redundancy Code (CRC) captured from the Color Graphics card video. The micro also compares the line number in the synchronization sequence and LCNT data to check the proper frame synchronization. The best CR word that provides reliable sampling is remembered by the micro and used for future sampling of real video data. The micro can set the line count register to capture a given line. This is useful because the micro may wish to capture only part of the given picture. For example, for the Color Graphics card only every other line need be captured because that card presents the same video information on successive pairs of lines. Another mode, required when the micro is not fast enough to capture successive lines, is to capture the next line you can and make the line number of that line available to the micro. A mode in which the VCF can capture only lines whose line number is divisible by a given integer is also useful in case a scaled-down presentation of the picture is desired. This technique requires that a user who wishes to run programs that require the predecessor display adapter either buy the predecessor or have one already. If the user has one already, he can dispose of the monitor (unless the monitor is compatible with the new display adapter, in which case compatibility can be achieved by switching the monitor between display adapters). There is no question of incompatibility because the old adapter is still present. The amount of additional hardware on the new adapter is minimal. The approach disclosed here minimizes the cost of the new adapter, but users who don't have the old adapter must buy both the old one and the new one. The technique herein described means that the system offers "simultaneous" compatibility: that both pictures from old programs and from new programs can be seen at the same time on the same screen, and in fact can be changing simultaneously. The response time for picture updates with old programs is substantially longer: time is added for the capture and reformatting of the picture.

A rough estimate based on a proposed adapter structure showed that between 1/6 and 1/4 of a second would be added to the picture update time for the Color Graphics card because of the VCF. This may mean that some highly animated applications (e.g., games) will not run satisfactorily. The use of VCF for the Color Graphics card has been discussed here only as an example. In fact, any digital video can be captured this way: say, from a high-resolution display generator, or from a text generator. Further, if a video analog-to-digital converter is used, video from an analog RGB source can be captured. If an NTSC-to-RGB converter is used, live TV can be captured, although if the TV picture is changing fast, then the resultant picture will be somewhat corrupted. The technique disclosed herein is similar to that employed in the Tektronix 4612 and 4632 video hard copy units. If differs primarily in the movement of captured video through the micro to the frame buffer, and in the way the sampling clock is established. The intent of the invention to support fast screen update is also quite different. What is disclosed here is a way to achieve flexible simultaneous compatibility with existing video sources. Minimal hardware on the new display adapter is required, although the old display adapter must be retained. The essentials of the technique are the VCF structure (the line counter, the sampling clock, and the shift register), the participation of the micro in transforming the pixel data before writing it into its frame buffer, and the technique for recovery of phase from the incoming video signal.

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DISCLOSURE TITLE: Variable Scale Vertical Expansion for Flat Panels

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DISCLOSURE TEXT:

This document contains drawings, formulas, and/or symbols that will not appear on line. Request hardcopy from ITIRC for complete article. Disclosed is a method for enabling vertical screen expansion, which is required when existing low resolution display mode is displayed on a high resolution LCD panel, at a variable expansion scale. No additional mechanism is required to an existing video chip and therefore the size, complexity, and the cost of the video subsystem may be significantly reduced while providing a good front-of-screen quality. Two different algorithms are provided for the graphics modes and the text modes to get better front-of-screen quality. Additionally, there is an option which enables to adjust the position of the displayed screen area on Flat Panel, when displayed screen resolution is smaller than panel resolution. Unlike CRT monitors, flat panels have a fixed number of pixels (e.g., 640x480, 800x600 or 1024x768 pixels). Lower resolution software running on a higher resolution panel only partially fills the totally usable display area. For instance, VGA 640x480 software displayed on XGA 1024x768 panel would leave 384 pixels horizontally and leave 288 lines vertically on the panel. To increase the usable display area when running lower resolution software on higher resolution panel, the screen must be expanded both horizontally and vertically. This invention enables the vertical expansion at a variable expansion scale rate.

In general, three methods are considered for the vertical expansion. o Expansion inside the video chip o RGB regeneration outside the video chip by using frame buffer o Expansion inside the Flat Panel Some video chips have a control logic which controls both CRT display timing and Flat Panel display timing with vertical expansion (Fig. 1). However, because Flat Panel has different display timing from CRT, the resolution on CRT is changed in the CRT/Flat Panel simultaneous display mode, compared with the CRT only mode. CRT can not retain original display mode resolution, when it is used in the simultaneous display mode with Flat Panel.

Another method is to capture the RGB data from the video chip and, then, regenerate the RGB data onto Flat Panel with vertical expansion and with different timing. Fig. 2 shows its mechanism. The generated RGB data, which is the output data of the video chip and the input data to the DAC for CRT, is captured by the RGB Capturing Logic at first. Then, the RGB data is stored to the frame memory, temporary. Secondly, the stored RGB data is read by the RGB Regeneration Logic with the different timing to display on high resolution Flat Panel. In this case, no resolution difference is observed on CRT screen between in the CRT only mode and in the CRT/Flat Panel simultaneous display mode. However, very complex logic and frame memory is additionally required for this buffering.

The last method is to make vertical expansion inside the Flat Panel (Fig. 3). In

this case, no resolution difference is observed on CRT screen between in the CRT only mode and in the CRT/Flat Panel simultaneous display mode and no additional logic or memory is required. Although no Flat Panels supports the vertical expansion, DTI Flat Panel is the only panel which has Dual Line operation. Dual Line operation is a capability to activate two horizontal lines on the panel at the same time by controlling the input signal, named Dual Line. Each horizontal line could be replicated by controlling this Dual Line signal. The vertical expansion method of this invention utilizes this DTI Flat Panel feature.

Fig. 4 summarizes the disadvantage of the conventional methods. The method of this invention provides a means for vertically expanding the low resolution display modes onto a high resolution Flat Panel at variable scaling rate. No additional memory is required to control Flat Panel, and CRT screen resolution is not affected even in the simultaneous display mode. This method is composed of the following steps. Step1: Expansion Rate Determination Step2: Vertical Expansion Step3: Display Area Vertical Adjustment In Step1, the panel height is compared with the vertical resolution of the current display mode. When the panel height (PNLH) is greater than the vertical resolution of the current display mode (DSPH) and smaller than 2*DSPH, then, Vertical expansion in Step2 occurred and the Dual Line signal is controlled based on the vertical expansion algorithm. If PNLH is greater than 2*DSPH, then the Dual Line signal to the Flat Panel is always activated in Step2. In Step2, two expansion methods are provided. o Linear expansion for graphic mode o Non-Linear expansion for text mode The first Linear expansion is based on the Bresenham algorithm and mostly used in graphics mode. The second Non-Linear expansion is provided by specifying the position of the expanded line in each character cell. This expansion pattern is given by register. This significantly improves the legibility of a character. In Step3, when the expanded screen resolution is still smaller than the panel resolution, border lines are added to the expanded display area to fit the Flat Panel resolution. Border lines could be added to both the top (Top Margin) and the bottom (Bottom Margin) of the Flat Panel screen by partially reducing the vertical retrace time and, then, placing additional border lines. For instance, when 640x350 display mode is selected, whole lines are replicated on the panel, in other word, Dual Line signal is always active. Then, screen image is expanded to 700 lines vertically, in Step2. When Flat Panel is 1024x768 resolution, 68 lines should be filled with border Lines. The top margin register specifies the number of top border lines. When top margin value is 30, 38 border lines are automatically added at the bottom of the screen. This provides the flexibility to adjust the position of display area on Flat Panel. Fig. 5 illustrates the block diagram, and Fig. 6 illustrates the data flow of the present invention. Fig. 7 is the description of the Bresenham's line algorithm used for the linear expansion in the graphics mode of the present invention. In the algorithm, x corresponds to the vertical line position, and y corresponds to the panel height minus vertical resolution of current display mode. The sign (negative or positive) of the decision variable (d) determines whether the dual line signal to Flat Panel input pin is activated or not.

Fig. 8 illustrates an example of the linear expansion based on the Bresenham's algorithm in graphics mode of the present invention. In the case of vertical expansion of 640x480 mode onto 1024x768 Flat Panel, the panel height is compared to the vertical resolution of the display mode. In this case, 768-480=288 is calculated. Secondly, using the Bresenham's line algorithm, vertically 480 line image is expanded to the 768 line image by controlling the Dual Line signal to Flat Panel. call BRESENHAM(0, 0, 480, 288) As shown in Fig. 8, 480 line image is expanded to 768 line image by activating Dual Line signal every 3rd pixel.

Fig. 9 is the format of the vertical expansion pattern register used for the Non-Linear expansion in the text mode vertical expansion of the present invention. Note that the each register bits specify the vertical line positions where the Dual Line signal to Flat Panel is activated. Bit 0-Bit 15 Vertical Expansion Pattern Bit n specifies whether to replicate (n+1)th line of a character cell.

Bit n

0 Do not replicate (n+1)th line 1 Replicate (n+1)th line Fig. 10 illustrates an example of the non-linear expansion based on the vertical expansion pattern register in the text mode vertical expansion of the present invention.

In the case of VGA mode 2+ which is 720x400 resolution text mode and the character cell size is 9x16, onto the 1024x768 Flat Panel, this 400 lines' image is expanded

to 768 lines' image by using the vertical expansion pattern, in order to preserve the size of the character cell. As shown in Fig. 10, the legibility of the character is significantly improved by programming the appropriate value to the vertical expansion pattern register. Fig. 11 is the format of the Top Margin register defines the height of the top side border area.

Bit 0-Bit 7 Top Margin These bits are the eight low-order bits of the number of the extra scan lines padded at the top of the active picture area on the panel in units of one scan line. The values are assigned as follows. Top Margin (TM) is specified by register. Bottom Margin (BM) is calculated automatically, as shown in Fig. 12. BM = PNLH - DSPH - EXPL - TM PNLH : Panel Height DSPH : Vertical Resolution of the Current Display Mode EXPL : Number of Expanded Lines in Step2